UNITED STATES PATENT AND TRADEMARK OFFICE

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ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _05 November 2004_.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _9-17_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _9-17_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _11 August 1999_ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

Introduction

1.   This communication is in response to the Applicants' Amendment dated

November 5, 2004. Claims 1-8 and 18-22 were cancelled. Claims 9-17 of the

application are pending. This office action is made non-final in response to the Request

for Continued Examination.

Drawings

2.   The draft person has objected to the drawings; see a copy of Form PTO-948 sent

with Paper No. 5 for an explanation.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.

4.   The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

        1.   Determining the scope and contents of the prior art.
        2.   Ascertaining the differences between the prior art and the claims at issue.
        3.   Resolving the level of ordinary skill in the pertinent art.
        4.   Considering objective evidence present in the application indicating obviousness
                or nonobviousness.

5.   Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takahashi**

et al. (TA) (U.S. Patent 6,061,283) in view of **Lin (LI)** (U.S. Patent 6,421,251).

5.1   As per Claim 9, **TA** teaches an electronic design automation system for verifying a user

design (Fig 2A); comprising:

        a computing system including a central processing unit and memory for modeling the

user design in software (Fig. 2A; CL4, L67 to CL5, L46; CL1, L27-29); and

        an internal bus system coupled to the computing system (Fig 2A).

        TA teaches hardware logic coupled to the internal bus system and for modeling at least a

portion of the user design in hardware (Fig 2A, Item 22; CL3, L55-65). **TA** does not expressly

teach reconfigurable hardware logic coupled to the internal bus system and for modeling at least

a portion of the user design in hardware. **LI** teaches reconfigurable hardware logic coupled to

the internal bus system and for modeling at least a portion of the user design in hardware (CL18,

L40-43), as the reconfigurable hardware can be programmably configured to model the hardware

portion of the user's electronic system design (CL18, L40-43). It would have been obvious to

one of ordinary skill in the art at the time of Applicants' invention to combine the method of **TA**

with the method of **LI** that included reconfigurable hardware logic coupled to the internal bus

system and for modeling at least a portion of the user design in hardware, as the reconfigurable

hardware could be programmably configured to model the hardware portion of the user's

electronic system design.

TA does not expressly teach control logic coupled to the internal bus system for

controlling the delivery of data between the reconfigurable hardware logic and the computing

system. **LI** teaches control logic coupled to the internal bus system for controlling the delivery

of data between the reconfigurable hardware logic and the computing system (CL12, L51-61), as

the that allows the entire circuit design to be modeled in software and the evaluation components

to be modeled in hardware (CL12, L53-56), so the system can simulate the circuit in software for

a time period and then accelerate the simulation in hardware (CL13, L10-11). It would have

been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine

the method of **TA** with the method of **LI** that included control logic coupled to the internal bus

system for controlling the delivery of data between the reconfigurable hardware logic and the

computing system, as the that would allow the entire circuit design to be modeled in software

and the evaluation components to be modeled in hardware, so the system could simulate the

circuit in software for a time period and then accelerate the simulation in hardware.

TA teaches VCD on-demand logic for recording a selected simulation session (CL2,

L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). TA does not

expressly teach VCD on-demand logic for recording at least a portion of a selected simulation

session range. **LI** teaches VCD on-demand logic for recording at least a portion of a selected

simulation session range (CL13, L9-12; CL13, L58-66), because the user can then perform analysis after simulation, by running the software simulation with input logs to the hardware model to compute the value change dump of all hardware components (CL42, L46-49) and the hardware accelerator can be used to simulate the data from the selected logging point to analyze the simulation results (CL21, L21-23). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **TA** with the method of **LI** that included VCD on-demand logic for recording at least a portion of a selected simulation session range, as the user could then perform analysis after simulation, by running the software simulation with input logs to the hardware model to compute the value change dump of all hardware components and the hardware accelerator could be used to simulate the data from the selected logging point to analyze the simulation results.

TA teaches dumping state information from the software model into a VCD file (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not expressly teach dumping state information from the hardware model into a VCD file. **LI** teaches dumping state information from the hardware model into a VCD file (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by running the simulation through the hardware model of the circuit design (CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **TA** with the method of **LI** that included dumping state information from the hardware model into a VCD file, as the hardware modeled design would provide high speed and the user could accelerate the test/debug process by running the simulation through the hardware model of the circuit design.

TA does not expressly teach dumping state information for a selected simulation target range, wherein the simulation target range is within the simulation session range. **LI** teaches dumping state information for a selected simulation target range, wherein the simulation target range is within the simulation session range (CL 13, L58 to CL14, L3; CL13, L9-12), because the user can then perform analysis after simulation, by running the software simulation with input logs to the hardware model to compute the value change dump of all hardware components (CL42, L46-49) and the hardware accelerator can be used to simulate the data from the selected logging point to analyze the simulation results (CL21, L21-23). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **TA** with the method of **LI** that included dumping state information for a selected simulation target range, wherein the simulation target range is within the simulation session range, as the user could then perform analysis after simulation, by running the software simulation with input logs to the hardware model to compute the value change dump of all hardware components and the hardware accelerator could be used to simulate the data from the selected logging point to analyze the simulation results.

TA does not expressly teach that the generated value change dump (VCD) file is dedicated to state information in the selected simulation target range and is exclusive of state information outside the selected simulation target range. **LI** teaches that the generated value change dump (VCD) file is dedicated to state information in the selected simulation target range and is exclusive of state information outside the selected simulation target range (CL13, L58 to 14L3; CL21, L16-23), because the user can then perform analysis after simulation, by running the software simulation with input logs to the hardware model to compute the value change

dump of all hardware components and the hardware accelerator can be used to simulate the data

from the selected logging point to analyze the simulation results (CL21, L17-23). It would have

been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine

the method of **TA** with the method of **LI** that included generated value change dump (VCD) file

being dedicated to state information in the selected simulation target range and being exclusive

of state information outside the selected simulation target range, as the user could then perform

analysis after simulation, by running the software simulation with input logs to the hardware

model to compute the value change dump of all hardware components and the hardware

accelerator could be used to simulate the data from the selected logging point to analyze the

simulation results.

Per Claim 10: **TA** teaches access logic for accessing the VCD file directly from

simulation time tl to debug the user design (CL2, L56-61; CL5, L36-46).

TA does not expressly teach first range selection logic for selecting a simulation session

range which begins at a simulation time t0 and ends at a simulation time t3. **LI** teaches first

range selection logic for selecting a simulation session range which begins at a simulation time

t0 and ends at a simulation time t3 (CL13, L60-64), as the selected session range affects the

simulation speed since the system must spend time and resources to record the output data to the

memory (CL21, L9-15). It would have been obvious to one of ordinary skill in the art at the time

of Applicants' invention to combine the system of **TA** with the system of **LI** that included first

range selection logic for selecting a simulation session range which begins at a simulation time

t0 and ends at a simulation time t3, as the selected session range would affect the simulation

speed since the system must spend time and resources to record the output data to the memory.

TA does not expressly teach second range selection logic for selecting a simulation target

range which begins at a simulation time t1 and ends at a simulation time t2, wherein the

simulation time t1 is greater than or equal to simulation time t0 and simulation time t2 is less

than or equal to simulation time t3. **LI** teaches second range selection logic for selecting a

simulation target range which begins at a simulation time t1 and ends at a simulation time t2,

wherein the simulation time t1 is greater than or equal to simulation time t0 and simulation time

t2 is less than or equal to simulation time t3 (CL13, L9-12), as the user can then perform analysis

after simulation, by running the software simulation with input logs to the hardware model to

compute the value change dump of all hardware components (CL42, L46-49) and the hardware

accelerator is used to simulate the data from the selected logging point to analyze the simulation

results (CL21, L21-23). It would have been obvious to one of ordinary skill in the art at the time

of Applicants' invention to combine the system of **TA** with the system of **LI** that included

second range selection logic for selecting a simulation target range which began at a simulation

time t1 and ended at a simulation time t2, wherein the simulation time t1 is greater than or equal

to simulation time t0 and simulation time t2 is less than or equal to simulation time t3, as the user

could then perform analysis after simulation, by running the software simulation with input logs

to the hardware model to compute the value change dump of all hardware components and the

hardware accelerator could be used to simulate the data from the selected logging point to

analyze the simulation results.

TA teaches dump logic for generating a VCD file of the software-modeled design (CL2,

L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not

expressly teach dump logic for generating a VCD file of the hardware-modeled design. **LI**

teaches dump logic for generating a VCD file of the hardware-modeled design (CL3, L56-62;

CL5, L34-40; CL18, L40-43), as the hardware modeled design provides high speed (CL3, L38-

39) and the user can accelerate the test/debug process by running the simulation through the

hardware model of the circuit design (CL20, L24-26). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to combine the system of **TA** with

the system of **LI** that included dump logic for generating a VCD file of the hardware-modeled

design, as the hardware modeled design would provide high speed and the user could accelerate

the test/debug process by running the simulation through the hardware model of the circuit

design.

TA does not expressly teach dump logic for generating a VCD file for the selected

simulation target range. **LI** teaches dump logic for generating a VCD file for the selected

simulation target range (CL13, L9-12), as the user can then perform analysis after simulation, by

running the software simulation with input logs to the hardware model to compute the value

change dump of all hardware components (CL42, L46-49) and the hardware accelerator is used

to simulate the data from the selected logging point to analyze the simulation results (CL21, L21-

23). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to combine the system of **TA** with the system of **LI** that included dump logic for

generating a VCD file for the selected simulation target range, as the user could then perform

analysis after simulation, by running the software simulation with input logs to the hardware

model to compute the value change dump of all hardware components and the hardware

accelerator could be used to simulate the data from the selected logging point to analyze the

simulation results.

Per Claim 11: **TA** teaches that the VCD on-demand logic further comprises test bench

process for providing primary inputs to the hardware-modeled design for evaluation (CL1, L32-

33); and

recording logic in the computing system for recording data associated with at least one

parameter in the simulation session rang (CL6, L9-13; CL6, L21-25).

Per Claim 12: **TA** teaches that the VCD on-demand logic further comprises process logic

in the computing system for loading the recorded data associated with at least one parameter

(CL6, L21-27).

TA teaches evaluation logic in the hardware logic for evaluating in the

hardware-modeled design the primary inputs from simulation time t0 to simulation time t2 (Fig

2A, Item 22; CL3, L55-65; CL6, L30-36). **TA** does not expressly teach evaluation logic in the

reconfigurable hardware logic for evaluating in the hardware-modeled design the primary inputs

from simulation time t0 to simulation time t2. **LI** teaches evaluation logic in the reconfigurable

hardware logic for evaluating in the hardware-modeled design the primary inputs from

simulation time t0 to simulation time t2 (CL18, L40-43), as the reconfigurable hardware can be

programmably configured to model the hardware portion of the user's electronic system design

(CL18, L40-43). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the system of **TA** with the system of **LI** that included

evaluation logic in the reconfigurable hardware logic for evaluating in the hardware-modeled

design the primary inputs from simulation time t0 to simulation time t2, as the reconfigurable

hardware could be programmably configured to model the hardware portion of the user's

electronic system design.

Per Claim 13: **TA** teaches the dump logic dumps the evaluated results from the

software-modeled design based on the primary inputs during the simulation into the VCD file

(CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does

not expressly teach the dump logic dumps the evaluated results from the hardware-modeled

design based on the primary inputs during the simulation into the VCD file. **LI** teaches the dump

logic dumps the evaluated results from the hardware-modeled design based on the primary inputs

during the simulation into the VCD file (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the

hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate the

test/debug process by running the simulation through the hardware model of the circuit design

(CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the system of **TA** with the system of **LI** that included the dump

logic dumping the evaluated results from the hardware-modeled design based on the primary

inputs during the simulation into the VCD file, as the hardware modeled design would provide

high speed and the user could accelerate the test/debug process by running the simulation

through the hardware model of the circuit design.

TA does not expressly teach the dump logic dumps the evaluated results based on the

primary inputs during the simulation target range into the VCD file. **LI** teaches the dump logic

dumps the evaluated results based on the primary inputs during the simulation target range into

the VCD file (CL13, L9-12), as the user can then perform analysis after simulation, by running

the software simulation with input logs to the hardware model to compute the value change

dump of all hardware components (CL42, L46-49) and the hardware accelerator is used to

simulate the data from the selected logging point to analyze the simulation results (CL21, L21-

23). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to combine the system of **TA** with the system of **LI** that included the dump logic

dumping the evaluated results based on the primary inputs during the simulation target range into

the VCD file, as the user could then perform analysis after simulation, by running the software

simulation with input logs to the hardware model to compute the value change dump of all

hardware components and the hardware accelerator could be used to simulate the data from the

selected logging point to analyze the simulation results.

6.   Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Takahashi et al. (TA) (U.S. Patent 6,061,283) in view of **Lin (LI)** (U.S. Patent 6,421,251) and

Parulkar et al. (PA) (U.S. Patent 6,363,509), and further in view of **Matsumura et al. (MA)**

(U.S. Patent 6,370,675).

6.1   As per Claim 14, **TA** and **LI** teach the system of Claim 13. **TA** does not expressly teach

compression logic for compressing the primary inputs and write logic for writing the compressed

primary inputs. **MA** teaches compression logic for compressing the primary inputs and write

logic for writing the compressed primary inputs (Abstract, L12-15; CL5, L55 to CL6, L10), as

the data after compression is stored in the memory (CL10, L54-56) and the memory required

will be reduced by compression. It would have been obvious to one of ordinary skill in the art at

the time of Applicants' invention to combine the system of **TA** with the system of **MA** that

included compression logic for compressing the primary inputs and write logic for writing the

compressed primary inputs, as the data after compression would be stored in the memory and the

memory required would be reduced by compression.

TA teaches write logic for writing state information from the software model (CL2, L56-

61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not expressly

write logic for writing state information from the hardware model. **LI** teaches write logic for

writing state information from the hardware model (CL3, L56-62; CL5, L34-40; CL18, L40-43),

as the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate

the test/debug process by running the simulation through the hardware model of the circuit

design (CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time

of Applicants' invention to combine the system of **TA** with the system of **LI** that included write

logic for writing state information from the hardware model, as the hardware modeled design

would provide high speed and the user could accelerate the test/debug process by running the

simulation through the hardware model of the circuit design.

TA does not expressly teach write logic for writing state information at simulation time

t0. **PA** teaches write logic for writing state information at simulation time t0 (CL10, L38-40),

because as per **LI** the user can select a particular point at which the simulation is desired; then

the user can select the start of session range which is recorded and simulate forward in time until

the simulation reaches the desired point so the post simulation analysis point is reached fast

(CL42, L23-45). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the system of **TA** with the system of **PA** that included write

logic for writing state information at simulation time t0, because the user could select a particular

point at which the simulation was desired; then the user could select the start of session range

which was recorded and simulate forward in time until the simulation reached the desired point

so the post simulation analysis point was reached fast.

Per Claim 15: **TA** teaches the process logic further comprises decompression logic for

decompressing the compressed primary inputs (CL2, L29-31); and

data transfer logic for delivering the decompressed primary inputs to the

hardware-modeled design for evaluation (CL1, L32-33; CL2, L31-33; Fig. 1, Blk17, 10 and 11).

7.   Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Takahashi et al. (TA) (U.S. Patent 6,061,283) in view of **Lin (LI)** (U.S. Patent 6,421,251), and

further in view of **Parulkar et al. (PA)** (U.S. Patent 6,363,509).

Per Claim 16: **TA** teaches write logic for writing the primary inputs (CL2, L54-60; CL1,

L39-43).

TA teaches write logic for writing state information from the software model (CL2, L56-

61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-25). **TA** does not expressly

write logic for writing state information from the hardware model. **LI** teaches write logic for

writing state information from the hardware model (CL3, L56-62; CL5, L34-40; CL18, L40-43),

as the hardware modeled design provides high speed (CL3, L38-39) and the user can accelerate

the test/debug process by running the simulation through the hardware model of the circuit

design (CL20, L24-26). It would have been obvious to one of ordinary skill in the art at the time

of Applicants' invention to combine the system of **TA** with the system of **LI** that included write

logic for writing state information from the hardware model, as the hardware modeled design

would provide high speed and the user could accelerate the test/debug process by running the

simulation through the hardware model of the circuit design.

      TA does not expressly teach write logic for writing state information at simulation time

t0. **PA** teaches write logic for writing state information at simulation time t0 (CL10, L38-40),

because as per **LI** the user can select a particular point at which the simulation is desired; then

the user can select the start of session range which is recorded and simulate forward in time until

the simulation reaches the desired point so the post simulation analysis point is reached fast

(CL42, L23-45). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the system of **TA** with the system of **PA** that included write

logic for writing state information at simulation time t0, because the user could select a particular

point at which the simulation was desired; then the user could select the start of session range

which was recorded and simulate forward in time until the simulation reached the desired point

so the post simulation analysis point was reached fast.

Per Claim 17: **TA** teaches state save logic for saving state information of the software

modeled design (CL2, L56-61; CL1, L27-29; CL4, L5-6; CL1, L62-65; CL5, L40-44; CL6, L21-

25). **TA** does not expressly teach state save logic for saving state information of the

hardware-modeled design. **LI** teaches state save logic for saving state information of the

hardware-modeled design (CL3, L56-62; CL5, L34-40; CL18, L40-43), as the hardware modeled

design provides high speed (CL3, L38-39) and the user can accelerate the test/debug process by

running the simulation through the hardware model of the circuit design (CL20, L24-26). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

combine the system of **TA** with the system of **LI** that included state save logic for saving state

information of the hardware-modeled design, as the hardware modeled design would provide

high speed and the user could accelerate the test/debug process by running the simulation

through the hardware model of the circuit design.

TA does not expressly teach state save logic for saving state information at simulation

time t0 in a first file and saving state information at simulation time t3 in a second file. **PA**

teaches state save logic for saving state information at simulation time t0 in a first file and saving

state information at simulation time t3 in a second file (CL10, L38-48), because as per **TI** the

user can select a particular point at which the simulation is desired; then the user can select the

start of session range which is recorded and simulate forward in time until the simulation reaches

the desired point so the post simulation analysis point is reached fast (CL42, L23-45). It would

have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

combine the system of **TA** with the system of **PA** that included state save logic for saving state

information at simulation time t0 in a first file and saving state information at simulation time t3

in a second file, because the user could select a particular point at which the simulation is

desired; then the user could select the start of session range which was recorded and simulate

forward in time until the simulation reached the desired point so the post simulation analysis

point was reached fast.

Response to Amendments

8.   Applicants' arguments, filed on November 5, 2004 have been fully considered.

Applicants' arguments, filed on November 5, 2004 under 35 U.S.C. 103 (a) are not persuasive.

9.   Examiner's response to the Applicants' arguments re presented below.

9.1   As per the applicants' argument that "while the VCD file can be used to generate and

evaluate the test pattern, there is no discussion in TA of the selection of a simulation session

range, or a target session range within the simulation session range; moreover, the VCD file in

TA is not used by the operator for debugging purposes, ... but is rather used for assembling and

evaluating the test patterns which are to be applied to the fabricated IC; since the test patterns are

intended as a global tool for testing the operation of the IC in virtually all conditions and with all

combinations of inputs, there would be no value to selectively targeting ranges, and ranges

within ranges, or to generating a VCD file dedicated to state information in the selected

simulation target range and being exclusive of state information outside said selected simulation

target range as is presently claimed; TA neither contemplates this type of approach, nor has any

use for it; LI discusses logging frequency in support of VCD, but only mentions that this

frequency can be adjusted; there is no discussion of selection of simulation ranges, or target

ranges, or of generating VCD files dedicated the state information in the selected simulation

target range", the Examiner respectfully disagrees.

LI teaches simulation session and logging selected values and states during the session

(CL13, L58-63). LI teaches dumping state information for a selected simulation target range,

wherein the simulation target range is within the simulation session range (CL 13, L58 to CL14,

L3; CL13, L9-12), because the user can then perform analysis after simulation, by running the

software simulation with input logs to the hardware model to compute the value change dump of

all hardware components (CL42, L46-49) and the hardware accelerator can be used to simulate

the data from the selected logging point to analyze the simulation results (CL21, L21-23). LI

uses the VCD file for analyzing the results from the selected logging point and target range

(CL21, L20-23). It is obvious that the analysis of the results is done as part of testing and

debugging the software simulation model.

Conclusion

10.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

571-272-3717. The examiner can normally be reached on Monday through Friday from
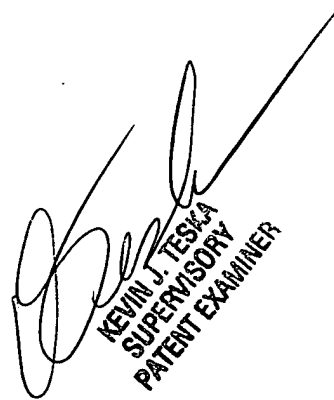
8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-305-

9600.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 5, 2005